

REMARKS

This is a full and timely response to the outstanding Office Action mailed March 17, 2009. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

1. **Response to Objection of Abstract**

The Office Action objects to the abstract of the disclosure for various informalities. The abstract has been amended to address the Examiner's concerns. Withdrawal of the objection is respectfully requested.

2. **Response to Objection of Title**

The title of the application has been objected to as allegedly not being descriptive. Applicant respectfully traverses the objection.

37 CFR § 1.72 simply states that the "title of the invention may not exceed 500 characters in length and must be as short and specific as possible." Accordingly, Applicants respectfully submit that the title "A Semiconductor Device with Metallic Electrodes and A Method for Use in Forming Such a Device" complies with the rule. For example, claim 1 recites a "semiconductor device comprising: a first electrode component; a second electrode component . . . wherein the first and second electrode components comprise electro-deposited metal" which specifically corresponds to the present title, "A Semiconductor Device with Metallic Electrodes and A Method for Use in Forming Such a Device." Accordingly, withdrawal of the objection to the title is respectfully requested.

3. **Response to Rejection of Claims under 35 U.S.C. § 112**

The Office Action rejects claim 14 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for having insufficient antecedent basis for the term "dielectric material." The claim has been amended to address the Examiner's concerns. Withdrawal of the rejection is respectfully requested.

4. Response to Rejection of Claims under 35 U.S.C. § 102 in view of Aratani

The Office Action rejects claims 1, 5, and 7-9 under 35 U.S.C. § 102(b) as allegedly being anticipated by *Aratani* (U.S. Patent No. 5,705,826).

a. Claim 1

As provided in independent claim 1, Applicant claims:

A semiconductor device comprising:
a first electrode component;
a second electrode component;
a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component;
a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components; and
a third layer comprising a substrate,
wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer,
wherein the first and second electrode components comprise electro-deposited metal,
wherein the device is a thin film transistor having a channel in the semiconductor material, a source electrode as the first electrode, a drain electrode as the second electrode, and a gate electrode,
wherein the source, drain and gate electrodes are formed from electro-deposited metal, and
wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer, the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer.

(Emphasis added).

Applicant respectfully submits that independent claim 1 is allowable for at least the reason that *Aratani* does not disclose, teach, or suggest at least “wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer, the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer,” as emphasized above.

As shown In FIG. 2 of *Aratani*, a continuous dielectric layer is not disclosed between gate electrode 2 and substrate 1. For at least this reason, *Aratani* does not teach or suggest at least “wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer, the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer,” as recited in claim 1.

Therefore, claim 1 is patentable over *Aratani*, and the rejection should be withdrawn.

b. Claims 1, 5, and 7-9

Claim 9 has been canceled without prejudice, waiver, or disclaimer. Dependent claims 1, 5, and 7-8 (which depend from independent claim 1) are allowable as a matter of law for at least the reason that the dependent claims 1, 5, and 7-8 contain all the features of allowable independent claim 1. For at least this reason, the rejection of claims 1, 5, and 7-8 should be withdrawn.

5. Response to Rejection of Claims under 35 U.S.C. § 102 in view of Yamazaki

The Office Action rejects claims 1, 9, 10, 14, and 24 under 35 U.S.C. § 102(b) as allegedly being anticipated by *Yamazaki* (U.S. Patent No. 6,013,930).

a. Claim 1

As provided in independent claim 1, Applicant claims:

A semiconductor device comprising:
a first electrode component;
a second electrode component;
a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component;
a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components; and
a third layer comprising a substrate,

wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer,

wherein the first and second electrode components comprise electro-deposited metal,

wherein the device is a thin film transistor having a channel in the semiconductor material, a source electrode as the first electrode, a drain electrode as the second electrode, and a gate electrode,

wherein the source, drain and gate electrodes are formed from electro-deposited metal, and

wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer, the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer.

(Emphasis added).

Applicant respectfully submits that independent claim 1 is allowable for at least the reason that *Yamazaki* does not disclose, teach, or suggest at least “wherein the source, drain and gate electrodes are formed from electro-deposited metal,” as emphasized above.

Yamazaki discloses that source electrode 112, drain electrode 113, and gate electrode 103 are “formed” but does not disclose that the electrodes are formed from electro-deposited metal. For at least this reason, *Yamazaki* does not teach or suggest at least “wherein the source, drain and gate electrodes are formed from electro-deposited metal,” as recited in claim 1. For example, *Yamazaki* discloses a laminate film of Titanium and/or Aluminum being used to form a source and drain electrodes which is not structurally the same as an electro-deposited metal. Col. 11, lines 58—63.

Therefore, claim 1 is patentable over *Yamazaki*, and the rejection should be withdrawn.

b. Claims 9, 10, 14, and 24

Claims 9-10 have been canceled without prejudice, waiver, or disclaimer. Dependent claims 14 and 24 (which depend from independent claim 1) are allowable as a matter of law for at least the reason that the dependent claims 14 and 24 contain all the features of allowable independent claim 1. For at least this reason, the rejection of claims 14 and 24 should be withdrawn.

6. Response to Rejection of Claims under 35 U.S.C. § 102 in view of Yamazaki

The Office Action rejects claims 1, 9, 18, 19, 22, and 23 under 35 U.S.C. § 102(b) as allegedly being anticipated by *Noguchi* (U.S. Patent No. 5,183,780).

a. Claim 1

As provided in independent claim 1, Applicant claims:

A semiconductor device comprising:

a first electrode component;

a second electrode component;

a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component;

a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components; and

a third layer comprising a substrate,

wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer,

wherein the first and second electrode components comprise electro-deposited metal,

wherein the device is a thin film transistor having a channel in the semiconductor material, a source electrode as the first electrode, a drain electrode as the second electrode, and a gate electrode,

wherein the source, drain and gate electrodes are formed from electro-deposited metal, and

wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer, the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer.

(Emphasis added).

Applicant respectfully submits that independent claim 1 is allowable for at least the reason that *Noguchi* does not disclose, teach, or suggest at least “a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components” and “wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer, the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer,” as emphasized above.

As shown in FIG. 4G, *Noguchi* discloses semiconductor film 21 separate from and not in contact with source electrode 28 and drain electrode 29. Further, *Noguchi* discloses the gate electrode being on the same layer as source and drain electrodes 28, 29. For at least this reason, *Noguchi* does not teach or suggest at least “a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components” and “wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer, the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer,” as recited in claim 1.

Therefore, claim 1 is patentable over *Noguchi*, and the rejection should be withdrawn.

b. Claim 18

As provided in independent claim 18, Applicant claims:

A semiconductor device comprising:
a first electrode component;
a second electrode component;
a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component;
a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components; and
a third layer comprising a substrate,
wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer,
wherein the first and second electrode components comprise electro-deposited metal,
wherein the device is a thin film transistor having a channel in the semiconductor material, a source electrode as the first electrode, a drain electrode as the second electrode, and a gate electrode,
wherein the source, drain and gate electrodes are formed from electro-deposited metal, and
wherein the first layer comprises a first portion of the source electrode, a first portion of the drain electrode and the gate electrode.

(Emphasis added).

Applicant respectfully submits that independent claim 18 is allowable for at least the reason that *Noguchi* does not disclose, teach, or suggest at least “a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components,” as emphasized above.

As shown in FIG. 4G, *Noguchi* discloses semiconductor film 21 separate from and not in contact with source electrode 28 and drain electrode 29. For at least this reason, *Noguchi* does not teach or suggest at least “a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components,” as recited in claim 18.

Therefore, claim 18 is patentable over *Noguchi*, and the rejection should be withdrawn.

c. Claims 19 and 22-23

Dependent claims 19 and 22-23 (which depend from independent claim 18) are allowable as a matter of law for at least the reason that the dependent claims 19 and 22-23 contain all the features of allowable independent claim 18. For at least this reason, the rejection of claims 19 and 22-23 should be withdrawn.

7. Response to Double Patenting Rejection of Claims

Claims 1, 5-6, 9, 18-19, and 22-23 have been rejected on the ground of nonstatutory obviousness-type double patenting as allegedly being unpatentable over claims 1-2, 5-6, 8-9, and 25 of copending U.S. Patent Application No. 10/563,679.

Applicants acknowledge the double patenting rejection and will respond to the rejection upon an indication of allowability of the non-canceled claims, thereby deferring payment of the statutory fee for a terminal disclaimer.

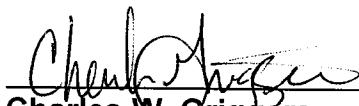
8. Cancellation of Claims

Claims 9-10, 25, 29, 31, 35-36, 42, 44, and 49 are canceled without prejudice, waiver, or disclaimer, and therefore, the rejection to these claims are rendered moot. Applicant takes this action merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicant reserves the right to pursue the subject matter of these canceled claims in a continuing application, if Applicant so chooses, and does not intend to dedicate any of the canceled subject matter to the public.

CONCLUSION

For at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,



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